Quality Reconfigurable Data Converters Using Inexpensive Digital Components

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Abstract: A/D and D/A converters have always dominated the mixed mode design cost. Price rises exponentially with bit precision. Complex, fast and accurate systems can be realized by digital methods, which are remarkably simple to implement and robust in nature. So why not replace a complete mixed mode design [1], with a cheap FPGA (i.e. Spartan 3E, price $8) that will also give you an instant option of reconfiguration to a higher specification in the future?

1 Introduction and the Data Converters Design Constraints

There are two types of converters, the Nyquist rate and the oversampled. The tendency is to use the former because of one-to-one association between the input and output and each sample is processed separately. A precision matched resistor ladder network is used to convert a digital word consisting of bits b_1, b_2, b_3-----b_N of a Nyquist rate DAC. The ideal digital to analogue conversion is given by the following equation**.**

$$Vout = Vref(b_1\, 2^{-1} + b_2\, 2^{-2} + ---+b_N\, 2^{-N}) \text{ ----------Eq1}$$

The percentage error can be worked out between the measured value and the ideal value in Eq1 and it should be below 0.5 LSB. Thus far the IC manufacturer's processes cannot match the ladder network resistors better than 0.02% precision. Therefore $2^{-N} \approx 0.02\%$ [2]

That works out ENOB (N) of about 12. Thus the limitation for the Nyquist type converter is 12 bits precision. If the required precision is more than 12 bits then the manufacturers have to use integrating converters. However they require at least 2^N clocks (N = bit resolution) to convert a single sample and therefore too slow for many applications.

2. The Delta-Sigma Converters

Enter the world of oversampling, Delta-Sigma converters and possibilities of having high resolution, desirable signal to noise ratio, respectable dynamic range, low costs and reconfigureability are certain realities. The technique has been known for number of years but the low operating speed of the components has been the hindrance to its development until now. As the clock speed of FPGAs are approaching 550 MHz (i.e. Xilinx Virtex5), the high-speed converters rivalling the Nyquist type but having much higher resolution is potentially an achievable target (i.e. 32 bit audio delta-sigma converters [3]).

3. Basic $\Delta\sum$ Modulator Theory and It's Noise Shaping and Resolution Analysis

Baseband signal processing is considered (i.e. signals with spectra from dc) in this discussion and particular attention is paid to the modulators, which are the heart of the operation in both the oversampling ADCs and the DACs. A first order modulator (Figure 1) is analysed and the results are extrapolated to the multi order modulator systems.

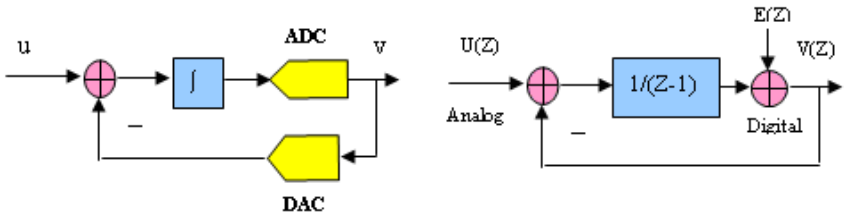

Figure 1: a) First order delta-sigma modulator b) A linear z-domain model of the modulator

The modulator consists of an adder, an integrator (also known as a loop filter), a non-precision ADC (i.e. comparator) and a DAC in the negative feedback. An approximate linear z-domain model is shown in the Figure 1b above. A digital output equation for the model can be simply written as follows.

$$v(n) = u(n-1) + e(n) - e(n-1) \text{ ----------Eq2}$$

As seen from Eq2, the digital output {v(n)} consist of an unaltered but delayed original analogue signal {u(n-1)} and differentiated version of quantisation error 'e'. The modulation process does not change the signal therefore

there is no in-band noise and distortion amplification. The differentiation of the error 'e' suppresses it further at lower frequencies. In general if loop filter (integrator) has high gain in the signal band, the quantisation noise is strongly attenuated known as the noise shaping process. The ADC non-linearity simply gets attenuated in-band with the quantisation error 'e'. The non-linearity in the feedback loop can be countered by using a 1-bit DAC. It can be shown that the L^{th} order modulator in-band noise power is given by (Eq3) [4] for OSR >> 1.

$$q^2 rms = \frac{\pi^{2L} e^2 rms}{(2L+1)(OSR)^{2L+1}} \text{ ----------Eq3}$$

Where OSR (Over sampling ratio) = $fs/2f_B$ {fs = sampling frequency, f_B = signal frequency}. The Eq3 does show that the in-band noise decreases with increasing OSR but the reduction is comparatively low for 1^{st} order modulator (L=1). For example, doubling of the OSR reduces the noise by 9 dB and improves ENOB only by 1.5 bits. Even for OSR = 256, ENOB < 13 bits provided 1 bit DAC is used in the feedback loop. A 2^{nd} order modulator (Figure 2a) will dramatically reduce the in-band noise as shown in Eq3 (L =2). For the second order modulators each doubling of the OSR will give additional 2.5 bit resolution. At OSR = 256, it will achieve ENOB of about 19 bits.

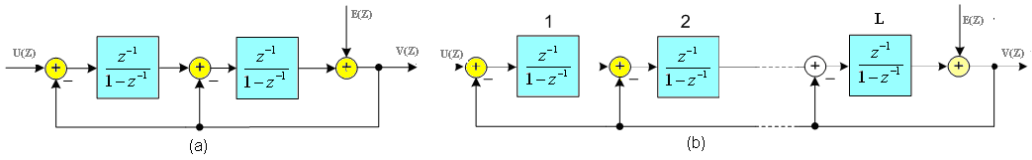

Figure 2: a) Second Order Delta-Sigma Modulator b) L^{th} Order Delta_Sigma Modulator

The above equation is theoretical derivations in reality a multi-order modulator will have lower resolution because of the stability considerations (i.e. ≈ 60 dB difference for 5^{th} order modulator) [5]). A plot of in-band noise versus OSR for up to 5th order modulator is shown below in Figure 3.

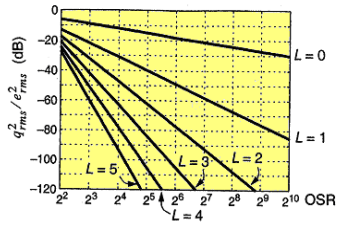

Figure 3: in-band noise versus OSR[Ref5]

It is obvious that a higher order modulator will need a smaller OSR to reduce the in-band noise.

The number of bits added to the resolution by doubling the OSR for the L^{th} order modulator is given by:
. (L + 0.5) bits----------Eq4 [5]

The dynamic range is given by the following equation [6].

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi 2L}\right)\left(2^N - 1\right)^2 M^{2L+1} \quad \text{----------Eq5}$$

Where L = Modulator Order, M = Over sampling Rate (OSR), N = Number Of Bits

The three most important design parameters for the converters have been mathematically defined, namely the in-band noise, the bit resolution and the dynamic range [Eq3, Eq4, Eq5]. Equipped with these tools, the reconfigurable data converter design can be implemented

4. A Reconfigurable Delta Sigma (ADC) Design

An attempt is made here to make the data converters fully digital and hence reconfigurable that is, no other hardware interface apart from no more than two resistors and two capacitor per i/o pin on the reprogrammable FPGAs (i.e. Xilinx FPGAs). In this respect the design of a delta sigma ADC will be a challenge, as an analogue signal needs to be interfaced to a digital i/o pin. A classic 1^{st} order $\Delta\sum$ ADC design is shown below in Figure 4(a), which consists of an adder, an integrator, a comparator, over-clocked flip flop and a feedback one bit DAC.

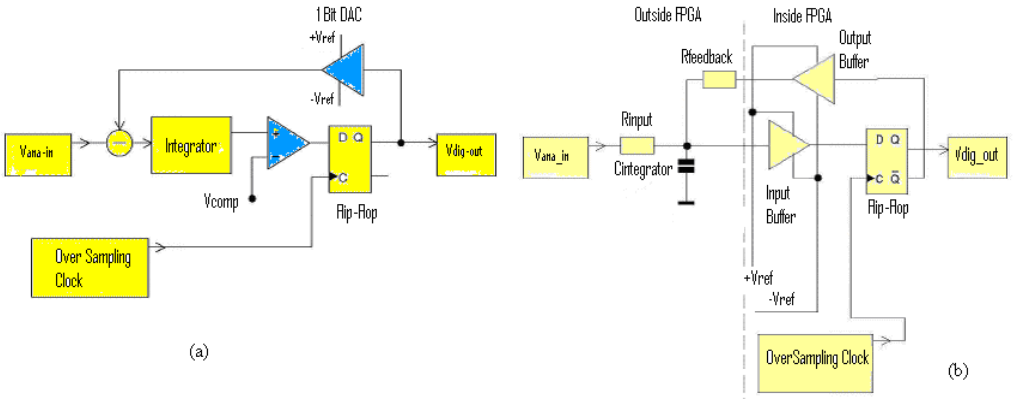

Figure 4: a) : 1st order Delta Sigma ADC Conventional Design b) 1st Order Delta Sigma ADC Implementation on the FPGA [7]

A proposed complete FPGA implement-able design is shown [7] in Figure 4(b). This design (Figure 4b) is a working system, which has been implemented in the G.712 PCM voice CODEC [7]. The plot in Figure 5 below shows the signal to noise ratio achieved with respect to G.712 [8] requirement specifications.

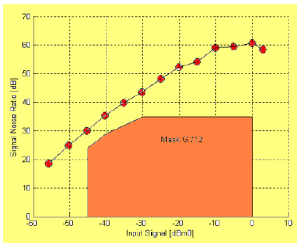

Figure 5: Signal to Noise Ratio Verses Input Level[7]

It is to note that using small voltage swings (25mV to 35mV) on the input capacitor ($C_{integrator}$- Figure 4b) for 3V3 CMOS type input buffer, result in an integrator characteristics, which is nearly identical to real integrator. So no special precautions will be required at the output. The 78dB voice codec 1st order ADC, will require clock frequency ratio of 512/1 {9 dB/Octave}. For a sample clock of 8KHz, the over-sampling clock will be 4.096 MHz. For the higher signal frequencies a second order modulator with three more passive components can be implemented (for the second integrator).

5. A Reconfigurable Delta Sigma DAC Design

A second order delta sigma DAC has been designed (Figure 6a). The input is a direct digital synthesized (DDS) tone of 7.99 MHz, 6 bits wide. The modulator sampling frequency is 192 MHz, thus an OSR=12. *The design in Figure 6a shows that only a resistor and two capacitors are used at the output pin of the FPGA, which makes up an AC coupled low pass filter to reconstruct an analogue output.*

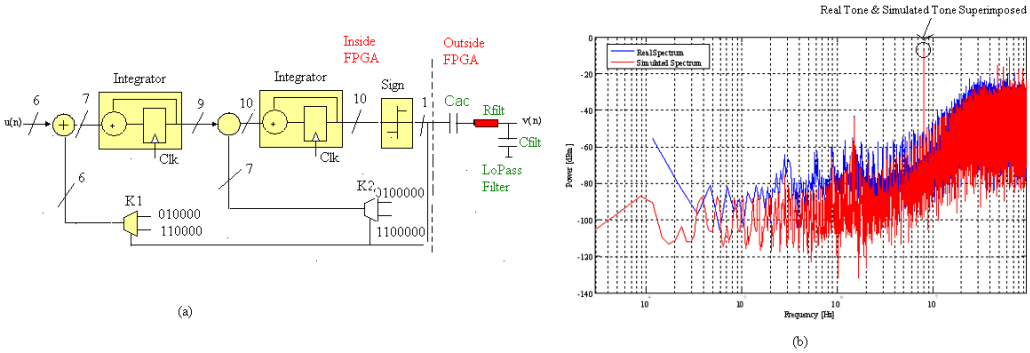

Figure 6: a) A FPGA implementation of DSM DAC b) A Matlab and an actual DS plot overlay for SNR versus sampling frequency

The table below shows the calculated values of the bit resolution and the SNR versus fs (sampling frequency in MHz) for the second order delta sigma DAC.

No	fs (MHz)	OSR	Resolution (Bits)	SNR (dB)
1	32	2	2.5	15
2	64	4	5.0	30
3	192	12	8.75	52.5

Table 1: Resolution and SNR Verses OSR

The input bit resolution is 6 bits and the DAC resolution is 8.75 bits at 192 MHz sample rate that means the input signal quality will not degrade. The requirement for the application SNR is about 44 dB, but the calculated value is 52.5 dB. A plot of the SNR versus sampling frequency was obtained and overlaid on the Matlab simulation for the second order modulator (Figure 6b). It shows that the in-band noise of the delta sigma DAC does have a slope of 40 dB /decade as expected but the SNR is about 50 dB that is 2 dB lower than the calculated value in Table 1 above. This is due to the fact that the clock signal in the FPGA has about 35.6ps (rms) of jitter (measured). The actual signal in the plot above is at 7.99MHz as expected.

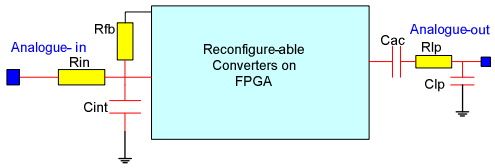

Figure 7: A Reconfigurable Converter Block on FPGA

6. Conclusion

With availability of high speed reprogrammable FPGAs, it is possible to design reconfigurable high performance data converters. The delta sigma converter are unbeatable on bit resolution [Ref 3] and with inherent capability of reducing the in-band noise [Figure 6b], a desired SNR can be achieved by simply selecting a correct combination of OSR and the order of the delta sigma modulators. Because of the oversampling requirements, the signal frequency is somewhat limited but still it is possible to handle signals in the order of few megahertz.

The Figure 7 is an example of how few passive components added to the I/O pins can be used to convert an ordinary signal path to a top of the range data converter and an updated program can be uploaded to achieve even better performance if required without any modifications to the existing hardware. As the mobile phones are more and more geared to handle multitude of functions, which will require data converters in many applications, the route taken here will enable the reuse of same hardware for even better performance. The data reconfigureability function will be even more useful in the spacecrafts where the hardware cannot be replaced but reloading the new configuration will keep the system up-to-date for years to come.

References.

[1] A Multibit Delta-Sigma Audio DAC with 120-dB Dynamic Range, I Fujimori, A Nogi, IEEE, vol.35, N°.8 Aug2000.

[2] Understanding Delta_Sigma Data Converters, R Schreier, G C Temes, page3.

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[4] Understanding Delta Sigma Data Converters, R Schreier, G C Temes , Page 9.

[5] Understanding Delta Sigma Data Converters, R Schreier, G C Temes , Page10.

[6] Sigma-Delta Data Converters: Sigma-Delta Data Converters Digital to Analog (DAC) Converter Theory, Design and Simulation Fernando Chavez

[7] Fully Digital Implemented Delta-Sigma Analog to Digital converter, Dr. Michael Gude & Gerriet Mueller Cologne Chip AG, Koeln (Cologne), Germany.

[8] ITU-T Recommendation G.712, "Transmission performance characteristics of pulse code modulation channels", ITU-T Study Group 15(2001-2004) 11/2001.

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