EE 231

Exam 3

November 19, 2008

Name: _____

Show all work. Partial credit will be given. No credit will be given if an answer appears with no supporting work.

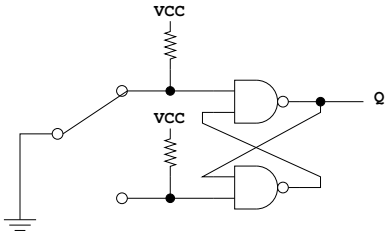
1. Circle the correct answer to questions (a) through (i); give a numerical answer for (j) and (k):

   (a) A movement of data from right (least significant bit) to left (most significant bit) is what type of shift:
   A. Right B. Left C. Parallel D. Finite state machine

   (b) A serial shift register with non-complemented feedback from the output of the last flip-flop to the input of the first is called a:
   A. Binary Counter B. Gray Code Counter C. Johnson Counter D. Ring Counter

   (c) A finite state machine in which the output depends on the present state and the present inputs is called a:
   A. Mealy machine B. Mannie machine C. Moore machine D. Vending machine

   (d) A finite state machine in which the output depends only on the present state is called a:
   A. Mealy machine B. Mannie machine C. Moore machine D. Vending machine



   (e) The circuit shown above is used for what purpose?
   A. Counter B. Pulser C. Shift register D. Switch debounce

   (f) The multiplexer is an example of what type of Boolean circuit?
   A. Sequential B. Combinational C. Moore machine D. Analog

   (g) Which sequential device has an output that is only dependent on the level of the inputs?
   A. Latch B. Multiplexer C. Flip-Flop D. Clock Tree

```
module ex3 (input clock, clear, load, x, output reg y)

always @(posedge clock, negedge clear)
    if (clear == 1'b0) y <= 0;
    else if (load == 1'b0) y <= x;
    else y <= y;

endmodule
```

(h) For the Verilog code above, what type on input is `clear`?
A. Latched B. Synchronous C. Asynchronous D. Tri-state

```
module ex3 (input clock, clear, x, output reg y)

always @(posedge clock, negedge clear)
    if (clear == 1'b0) y <= 0;
    else if (load == 1'b0) y <= x;
    else y <= y;

endmodule
```

(i) For the Verilog code above, what type on input is `load`?
A. Latched B. Synchronous C. Asynchronous D. Tri-state

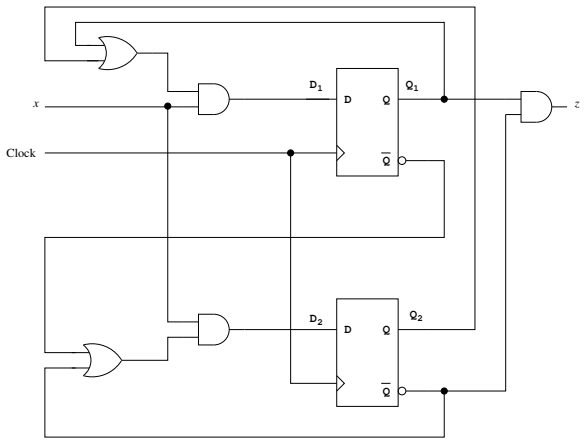
(j) A finite state machine has eleven states. (The number of states cannot be reduced.) What is the minimum number of flip-flops needed in the state register?

(k) A finite state machine has eleven states. (The number of states cannot be reduced.) What is the number of flip-flops needed in the state register if the design is done using one-hot assignment?

2. A traffic signal controller has two inputs (plus a clock) and three outputs. The inputs are E (for east-west traffic) and N (for north-south traffic). The outputs are R (red light), Y (yellow light) and G (green light). The system is to behave as follows: G will be high for two clock cycles. If E is high on the second clock cycle, G will stay high for one more clock cycle. After this, Y will go high for one clock cycle, then R will go high for two clock cycles. If N is high on the second R-high clock cycle, R will stay high for one more clock cycle. After this, R and Y will go high at the same time, then the system will go back to the start of the sequence.

   Draw a state diagram for this system.

3. Consider the circuit below.



(a) Is this a Mealy or a Moore machine? Why?

(b) Write Boolean equations for the flip-flop inputs D_1 and D_2 and the system output z.

(c) Tabulate the state transition table for the circuit.

(d) Draw a state diagram for the system.

4. The Verilog code program below describes a universal counter:

```
module ucntr( input clk, clear, ena, dir, load,
              input [3:0] D,
              output reg [3:0] Q);

always @(posedge clk)
    if (clear) Q <= 4'h0;
    else if (load) Q <= D;
    else if (ena & dir) Q <= Q + 4'h1;
    else if (ena & ~dir) Q <= Q - 4'h1;
    else Q <= Q;
endmodule
```

Show what will be on the output Q for the following inputs: