

**EE 231 – Homework 5**  
**Due September 30, 2009**

1. For the circuit shown in Fig. 4.25 (page 153 of the text),
  - (a) Write the Boolean function for the output in terms of the input variables.
  - (b) If the circuit is listed in a truth table, how many rows and columns would there be in the table?
  - (c) Write a Verilog dataflow model for the circuit.
2. A minority circuit is a circuit with an odd number of inputs whose output is a 1 if and only if a minority of its inputs are 1.
  - (a) Find the truth table for a three-input minority circuit.
  - (b) From the truth table, find the Boolean equation for the circuit.
  - (c) Write a Verilog dataflow model of the circuit.
3. Problem 4.10. Treat this as a 4-input, 4-output combinational circuit, find the truth table, and use Karnaugh maps to simplify.
4.
  - (a) Design a full subtractor circuit with three inputs  $x$ ,  $y$ ,  $B_{in}$ , and two outputs  $D$  and  $B_{out}$ . The circuit subtracts  $x - y - B_{in}$ .  $B_{out}$  is 0 if no borrow is needed to complete the subtraction, and 1 if a borrow is needed.
  - (b) Draw a block diagram showing how four full subtractors can be used to implement a 4-bit subtraction.
  - (c) Write a Verilog dataflow model to implement the circuit of Part (b).
5.
  - (a) The adder-subtractor circuit of Fig. 4.13 has the following values for mode input M and data inputs A and B:

	M	A	B
(a)	0	0110	0101
(b)	0	1100	1101
(c)	1	0110	0011
(d)	1	0000	0001

In each case determine the values of the four SUM outputs, the carry C, and overflow V.

- (b) Using the conditional operator (?), write a Verilog dataflow description of the four-bit adder-subtractor of Fig. 4.13.
6. For the circuit shown in Fig. 4.13 of the text, verify that the V output bit is correct for the addition operation. That is, show that (a) V will be 1 when you add two positive numbers together ( $B_3 = 0$  and  $A_3 = 0$ ) and get a negative number ( $S_3 = 1$ ), (b) V will be 1 when you add two negative numbers together ( $B_3 = 1$  and  $A_3 = 1$ ) and you get a positive number ( $S_3 = 0$ ), and (c) the V output will be 0 in all other circumstances (adding two positives and getting a positive, adding two negatives and getting a negative, or adding a positive and a negative number).

7. Assume that the exclusive-OR gate has a propagation delay of 15 ns and that the AND and OR gates have a propagation delay to 10 ns. What is the total propagation delay of the four-bit adder of Fig. 4.12?