EE 308 – Homework 6

Due Feb. 25, 2002

For all problems below assume your are using a 68HC912B32 chip with a 16 MHz crystal (which results in an 8 MHz timer clock).

1. Problem 4 on Page 239 of the text.
2. The prescaler bits are set to `PR2:0 = 011`. The first time the `TCNT` register is read the value is `0x2345`. The next time the `TCNT` register is read, the value is `0xCDEF`. Assuming the time between reads was less than the overflow period of the counter, how much time (in seconds) passed between the two reads?
3. The prescaler bits are set to `PR2:0 = 011`. The first time the `TCNT` register is read the value is `0xCDEF`. The next time the `TCNT` register is read, the value is `0x2345`. Assuming the time between reads was less than the overflow period of the counter, how much time (in seconds) passed between the two reads?
4. An HC12 has the following data in its memory:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
FFC0	CC	05	9F	CD	99	03	84	9C	01	9B	CC	90	66	FC	93	30
FFD0	7E	E3	4B	7E	E5	38	21	54	05	83	09	34	2A	38	3C	03
FFE0	41	38	66	F2	7C	13	37	0C	25	F2	0C	38	5F	1B	42	1A
FFF0	7A	26	21	13	6A	AA	20	1F	4B	38	33	38	45	38	10	20

   (a) What happens to the program counter when the HC12 is powered up or reset? What is the address of the first instruction the HC12 will execute after a reset?

   (b) What is the address of the first instruction the HC12 will execute when it receives a Timer Overflow interrupt?

   (c) What is the address of the first instruction the HC12 will execute when it receives a SPI interrupt?

   (d) What is the address of the first instruction the HC12 will execute when it receives a Real Time interrupt?

5. Below are the values of some timer registers in the HC12:

TSCR	TCTL1	TCTL2	TCTL3	TCTL4	TMSK1	TMSK2	TFLG1	TFLG2
80	A4	C2	5F	76	47	03	21	80

   (a) Is the Timer enabled?

   (b) Is the Timer Overflow Interrupt enabled?

   (c) Is the Timer Overflow Flag set?

   (d) What is the overflow time for the TCNT register?

6. Write some assembly language code which will enable the timer subsystem, set the timer overflow rate to 65.536 ms, and enable the timer overflow interrupt.

7. Write some C code which will enable the timer subsystem, set the timer overflow rate to 65.536 ms, and enable the timer overflow interrupt.

8. Answer the question from Part 5 of Lab 6.

9. Write the assembly language program for Part 6 of Lab 6.

10. Write the C program for Part 6 of Lab 6.