EE 308

Exam 3

May 4, 2009

Name: _____

You may use any of the Freescale data books, the class lecture notes, and a calculator. Show all work. Partial credit will be given. No credit will be given if an answer appears with no supporting work.

For all the problems in this exam, assume you are using an MS9S12 with an 8 MHz crystal, resulting in a 24 MHz bus clock.

Also, assume that `hcs12.h` has been included, so you can refer any register in the MC9S12 by name rather than by its address in any C code you write.

1. I^2C Bus

   (a) The schematic for the Dragon12-Plus board shows that the SDA and SCL lines of the I2C bus are connected to VCC through pull-up resistors. What are the purpose of these pull-up resistors?

   (b) Suppose you accidentally connected the pull-up resistors on SDA and SDL to ground rather than VCC. What would the signals on the SDA and SCL lines look like?

   (c) Describe a feature of the START condition that can be used to distinguish it from any other type of activity on the I2C bus.

   (d) The ADS7830 for Texas Instruments is an 8-bit, 8-channel A/D converter with an I2C bus. The data sheet for the ADS7830 says that, in standard mode, the SCL clock frequency should be less than 100 kHz. What value should you write to what register in order the set up the MC9S12 to run the I2C bus as fast as possible such that it is still compatible with the ADS7830? Explain.

2. A/D Converter

(a) Suppose the A/D converter on the MC9S12 is set up in 10-bit mode, with V_{RL} = 1.0 V and V_{RH} = 3.0 V. ATD0 of the MC9S12 is set up to convert all eight inputs, and store the results in right-justified mode. After a series of conversions, the following results are obtained:

ATD0DR0	ATD0DR1	ATD0DR2	ATD0DR3	ATD0DR4	ATD0DR5	ATD0DR6	ATD0DR7
0x0049	0x008D	0x036B	0x0116	0x0158	0x019E	0x01E2	0x026B

i. What was the input voltage on Channel 0?

ii. What was the input voltage on Channel 4?

(b) Write some C code to set up ATD0 to operate in 10-bit mode, and to convert Channels 0 through 3 one time, then stop.

(c) Write some C code to wait until the above set of 4 conversion has finished.

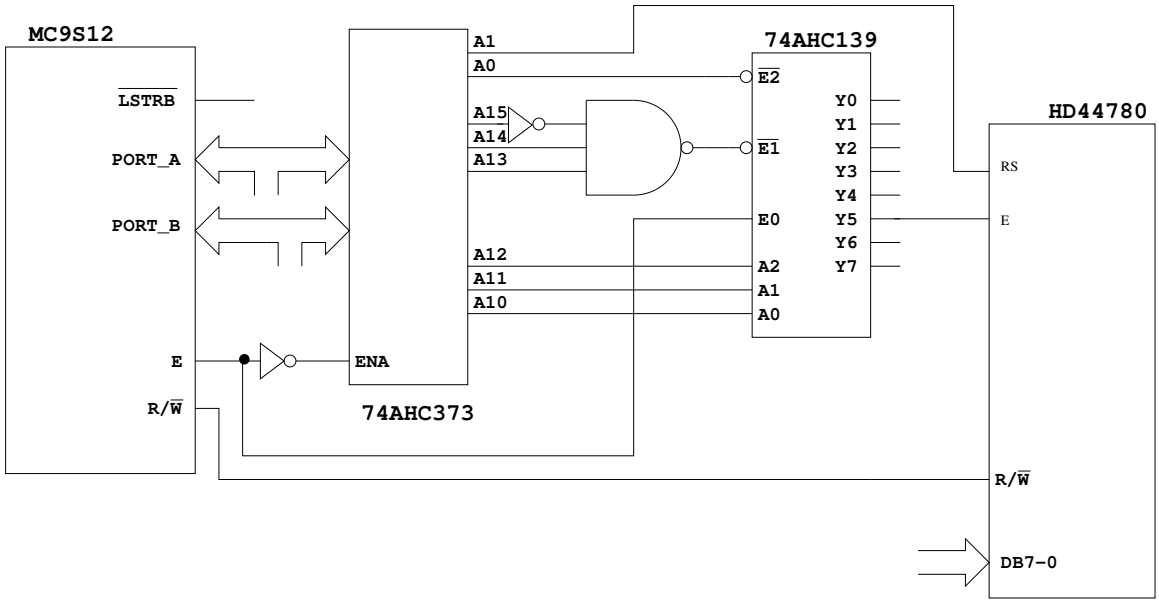
(d) Given your setup above, how long did it take the MC9S12 to convert the four channels?

3. Interfacing

   The Hitachi HD44780 is a chip to control LCD displays. The figure below shows a possible way to connect the HD44780 to an MC9S12.

   The HD44780 is enabled when its E input is high. (This is not the same as the E clock for the MC9S12.) The HD44780 has two internal register, Register 0 and Register 1. The RS input to the HD44780 is a register select. If RS is low, Register 0 is selected. If RS is high, Register 1 is selected. R/$\overline{\text{W}}$ is the Read/Write line. If R/$\overline{\text{W}}$ is high, the chip is in read mode. R/$\overline{\text{W}}$ is low, the chip is in write mode.

   The 74AHC139 is the same as the 74AHC138, except the selected output is active high rather than low. That is, when the chip is not enabled, all eight outputs are low. when the chip is enabled, The output corresponding to A_2 A_1 A_0 is high, and the other seven outputs are low. The 74AHC373 is an eight-bit transparent latch. When ENA is high, the data inputs are transfered into the data outputs. When ENA goes low, the data doesn't change even if the data inputs change.



   (a) For what range of addresses will the HD44780 be selected? Explain.

   (b) Should the data lines of the HC44780 be connected to Port A or Port B? Explain.

   (c) Explain how you can access Register 0, and how you can access Register 1.

(d) Write some C code which will write the 8-bit value 0xAA to Register 0.

(e) Write some C code which will read the 8-bit value from Register 1, and save it in a variable called `Reg_1`.

(f) The timing diagrams for the HC44780 chip are attached. Assume that the propagation delays through each glue logic chip is 2 ns. Is the time t_{AS} on the HC44780 data sheet compatible with an MC9S12 with a 24 MHz bus clock, and no E-clock stretches? If the time is not compatible, can you make it compatible by changing the bus clock frequency or adding E-clock stretches? Explain.

(g) Is the time t_{DSW} on the HC44780 data sheet compatible with an MC9S12 with a 24 MHz bus clock, and no E-clock stretches? If the time is not compatible, can you make it compatible by changing the bus clock frequency or adding E-clock stretches? Explain.