Digital Electronics
Spring, 2020
Lecture: on M W F, 11:00 – 11:50

Instructor: Sihua Shao
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Course Description: This course develops on a basic understanding, design, and simulation of digital systems. Topics include number systems, Boolean algebra, logic gates, truth tables, adder/subtractor, arithmetic operation, multiplexer, and code converter. The course also covers sequential digital design via finite state machines. Simulation-base projects provide exposure to computer-aided design and simulation of digital systems using Verilog.

Co-requisites: *EE 271 (Mathematical Engineering),* or *CSE 113 (Introduction to Programming),* or *ES 111 (Computer Programming for Engineers)*

Place in Curriculum: This course is open to majors and non-majors. The *EE 252 (Digital Electronics)* is a prerequisite to the *EE 361 (Mixed Electronics Lab I)*.

Course Learning Outcomes:
After completion of this course, students are expected to be able to:

- Explains number systems, logical functions, and the simplification of logical statements.
- Identify the adder, subtractor, and combinational circuit.
- Use flip-flops, counters, and registers.
- Design digital circuits and perform the correct testing and analysis.
- Conduct simulations to determine the performance of a digital system.
- Work with digital circuits and simulate the circuits to troubleshoot their operations.

Program Learning Outcomes: https://www.nmt.edu/academics/eleceng/undergrad/index.php

Course Requirements:
Textbook: *Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, Third Edition, McGraw-Hill, 2014*

Grading:

- Lecture: 65%
  - Homework: 20%
  - 2 Midterms: 15% each
  - Final term: 15%
- Simulation-based projects: 25%
- In-class quest: 10%

A	90-100	C	70-72
A-	86-89	C-	66-69
B+	83-85	D+	63-65
B	80-82	D	60-62
B-	76-79	F	<60
C+	73-75		

There will be no make-up exams except in the case of extraordinary circumstances. Homework is due one week after the assigned date (e.g., if homework 1 is assigned on Aug. 28, then it is due on Sep. 4). The simulation-based project is due 4 weeks after the assigned date. Students may work together on homework but must turn in individual assignments that CANNOT BE IDENTICAL.

Academic Honesty: New Mexico Tech's Academic Honesty Policy for undergraduate and graduate students is found in the student handbook, which can be found at: http://www.nmt.edu/student-handbook. You are responsible for knowing, understanding, and following this policy.

Reasonable Accommodations:
New Mexico Tech is committed to protecting the rights of individuals with disabilities. Qualified individuals who require reasonable accommodations are invited to make their needs known to the Office of Counseling and Disability Services (OCDS) as soon as possible. To schedule an appointment, please call 835-6619.

Counseling Services:
New Mexico Tech offers mental health and substance abuse counseling through the Office of Counseling and Disability Services. These confidential services are provided free of charge by licensed professionals. To schedule an appointment, please call 835-6619.

Respect Statement: New Mexico Tech supports freedom of expression within the parameters of a respectful learning environment. As stated in the New Mexico Tech Guide to Conduct and Citizenship: "New Mexico Tech's primary purpose is education, which includes teaching, research, discussion, learning, and service. An atmosphere of free and open inquiry is essential to the pursuit of education. Tech seeks to protect academic freedom and build on individual responsibility to create and maintain an academic atmosphere that is a purposeful, just, open, disciplined, and caring community."

Title IX Reporting:
Sexual misconduct, sexual violence and other forms of sexual misconduct and gender-based discrimination are contrary to the University's mission and core values, violate university policies, and may also violate state and federal law (Title IX). Faculty members are considered "Responsible Employees" and are required to report incidents of these prohibited behaviors. Any such reports should be directed to Tech's Title IX Coordinator (Dr. Peter Phaiah, 20D Brown Hall, 575-835-5187, titleixcoordinator@nmt.edu). Please visit Tech's Title IX Website (www.nmt.edu/titleix) for additional information and resources.

Tentative Lecture Schedule:

Date	Chapter	Topic
Jan. 13, 15, 17	Chap. 1	Digital Representation of Information
Jan. 20	Holiday	
Jan. 22, 24, 27, 29, 31	Chap. 2	Truth Table, Logic Gate, Boolean Algebra, Synthesis using SOP and POS forms, K-map
Feb. 3, 5, 7,	Chap. 2	Intro to Verilog, NAND and NOR Networks
Feb. 10, 12, 14	Chap. 4	Multiplexer and Code Converters
Feb. 17		Midterm 1 (Until Chap. 2)
Feb. 19, 21, 24	Chap. 3	Number Representation and Adder/Subtractor
Feb. 26, 28, Mar. 2	Chap. 5	Latch and Flip-flop
Mar. 4, 6, 9	Chap. 6	Sequential Circuit Design
Mar. 11, 13	Chap. 5	Register and Counter
Mar. 16 – 20	Holiday	
Mar. 23, 25, 27, 30	Chap. 5	Register and Counter
Apr. 1		Midterm 2 (Until Sequential Circuit Design)
Apr. 3, 6, 8	Chap. 5	Timing Analysis, Clock Skew
Apr. 10	Holiday	
Apr. 13, 15, 17	Appendix B	Logic Gate Implementation
Apr. 20, 22, 24	Chap. 5	Design Example: Reaction Timer
Apr. 27, 29		Final Term Review

Tentative Simulation-based Project Schedule:

Date	Topic
Jan. 27	Introduction to Verilog and Vivado
Feb. 14	Multiplexer and Decoder
Feb. 28	Adder/Subtractor and ALU
Mar. 13	Register and Counter
Mar. 30	CCU and Graphic Design of Processor